David Lee

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(347) 997 - 0902

Relevant Coursework
VLSI Design
Computer Architecture and Organization
Integrated Circuit Design
Graduate GPA: 3.667

Skills
Electronics
Arduino
Embedded Design
Lab Equipment
Schematic Capture
PCB Layout
Soldering

Software
Altium Designer
Vivado Suite
Cadence Virtuoso
OrCad Capture
PSpice
MatLab

Programming
Verilog
Python
Linux
C / C++
MATLAB

Language Fluency
English
Korean

Education

Northeastern University, Boston, MA

Bachelors of Science in Electrical Engineering — *May 2020*
Minor in Business Administration
Masters of Science in Electrical Engineering — *May 2022*
Concentration in Hardware and Software for Machine Intelligence

Regis High School, New York, NY — *May 2015*

Experience

Edwards Vacuum
Lead Electrical Systems Engineer — *January 2021 - Present*
- Lead Electrical Engineering team in development of New Product Innovations
- Execute projects from initial specification definition to production

R&D Electrical Engineer — *April 2020 - January 2021*
- Design and execute DVT's and RDT's to Semi Standards
- Design and test electrical subsystems used in vacuum pumps and compressors

Electrical Engineering Co-Op — *Jan 2018 - April 2020*
- Lead PCB schematic and layout design for NPI and sustaining projects
- Create and perform Design Verification tests to Semi compliance and reliability standards

Communications and Power Industries
Electrical Engineering Co-Op — *Jan 2017 - June 2017*

School Projects

32 Bit CLA Adder - VLSI Design
- Design and layout CMOS schematic and Layout of a Carry Look Ahead Adder and execute DRC and LVS checks
- Extract parasitic capacitance and resistance from layout and compare post layout simulation with ideal simulation

PUF Machine Learning Attack
- Research and use classification tools in MATLAB to attack the given Physically Uncloneable Function and predict Command and Response pairs

Single Cycle Datapath
- Utilized Icarus Verilog to program test benches and confirm functionality of single cycle datapath processor

Physics Hardware Acceleration
- Create a hardware accelerator with Vivado on PYNQ Z2 FPGA platform and verify the hardware speedup

Capstone: PLAN Tile
- Research and design floor tile embedded with LED matrix to detect and direct pedestrian foot traffic using frequency domain analysis

Other Work Experience

Eagles Tae Kwon Do Inc.
USA Olympic Tae Kwon Do Level 1 Coach — *Sept 2014 - Aug 2016*
- Coached potential and active USAT Junior Olympic Team athletes in National and International competitions